Docket No. 034299-688

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICANT:	Mickael Guibert et al.
SERIAL NO.:	10/574,315
FILING DATE:	March 30, 2006
TITLE:	COMPONENT WITH DYNAMICALLY RECONFIGURABLE ARCHITECTURE
EXAMINER:	(to be assigned)
ART UNIT:	(to be assigned)

CERTIFICATE OF MAILING

I hereby certify that this paper is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date printed below:

Date: 7-24-06 Name: Sharon E. Byam

Sharon E. Byam

Mail Stop: Amendment
COMMISSIONER FOR PATENTS
P.O. Box 1450
ALEXANDRIA, VA 22313-1450

INFORMATION DISCLOSURE STATEMENT

In compliance with the duty of disclosure under 37 C.F.R. §§ 1.56, 1.97 and 1.98, applicant hereby submits this Information Disclosure Statement (IDS) including a Form PTO-1449 containing a list of references which may be material to the examination of the above-referenced application. This submission is not to be construed as a representation that a prior art search has been conducted, that additional information material to the examination of this application does not exist, or that any one or more of the listed references constitutes prior art.

The Examiner is urged to carefully consider this Information Disclosure Statement and all the listed references, and to indicate same by initialing the appropriate portion(s) of the Form PTO-1449 and forwarding an initialed copy to applicant.

If this box ☒ is checked, this application was filed after June 30, 2003 and qualifies for the blanket waiver of deposit of copies of U.S. Patents and U.S. Patent Application Publications in accordance with the written waiver of 37 CFR §1.98 (a)(2)(i) Official Gazette Published in Official Gazette Notices of August 5, 2003 (1273OG55). Accordingly, such copies are not submitted.

I

This statement is filed pursuant to:

☒ **37 C.F.R. § 1.97(b).**

This information disclosure statement is filed either:

(1) within three months of the filing date of a national application other than a continued prosecution application under §1.53(d);

(2) within three months of the date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application;

(3) before the mailing date of a first office action on the merits; **or**

(4) before the mailing of a first office action after the filing of a Request for Continued Examination under 37 C.F.R. §1.114, **whichever event occurs last.**

Accordingly, this information disclosure statement requires no fee and no certification.

☐ **37 C.F.R. § 1.97(c).**

This information disclosure statement is filed **after** the period specified in 37 C.F.R. § 1.97(b), but **before** the mailing date of any of the following:

(1) a final action under 37 C.F.R. § 1.113;

(2) a notice of allowance under 37 C.F.R. § 1.311; **or**

(3) an action that otherwise closes prosecution in the application.

Accordingly, this information disclosure statement requires either:

(1) the fee specified in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c); **or**

(2) a certification according to 37 C.F.R. § 1.97 (e)(1) or (2).

☐ **37 C.F.R. § 1.97(d).**

This information disclosure statement is filed **after** the period specified in 37 C.F.R. § 1.97 (c).

Accordingly, this information disclosure statement requires:

(1) a certification in accordance with 37 C.F.R. § 1.97(e); **and**

(2) the fee specified in 37 C.F.R. § 1.17 (p) to consider an information disclosure statement under 37 C.F.R. § 1.97(d).

If this statement crosses in the mail with an office action, or is otherwise not in the indicated category of 37 C.F.R. §1.97, it is respectfully requested that this statement be treated in the next appropriate category and made of record. To the extent required, please treat this paper as a conditional petition for acceptance of the information disclosure statement.

II

Fees Due:

☒ No fee is due.

☐ The fee specified in 37 C.F.R. § 1.17(p) for submission of an information disclosure statement under 37 C.F.R. § 1.97(c) or 37 C.F.R. § 1.97(d) is enclosed (**$180**).

III

Certification:

☒ No certification is necessary.

☐ Pursuant to 37 C.F.R. § 1.97(e)(1), the undersigned hereby certifies:
That each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this information disclosure statement.

☐ Pursuant to 37 C.F.R. § 1.97(e)(2), the undersigned hereby certifies:
No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the undersigned after making reasonable inquiry, no item of information contained in this information disclosure statement was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this information disclosure statement.

IV

Please charge any additional required fee or credit any overpayment to our deposit account number 50-1698.

Respectfully submitted,
THELEN REID & PRIEST LLP

Dated: 7/24/01

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Form PTO-1449 (Rev. 2-32) U.S. Department of Commerce Patent and Trademark Office	Atty. Docket No. 034299-688	Serial No. 10/574,315
Information Disclosure Statement by Applicant	Applicant: Mickael Guibert et al.	
(Use several sheets if necessary)	Filed: March 30, 2005	Group: (to be assigned)

U.S. Patent Documents

Init.		Document No.	Date	Name	Class	Subclass	Filing Date
	A	5,892,962	04/06/99	Cloutier			
	B	6,150,839	11/21/00	New et al.			

Foreign Documents

Init.		Document No.	Date	Country	Class	Subclass	Translation Yes	Translation No

Other Documents (Including Author, Title, Date, Pertinent Pages, etc.)

	C	Altera, "Flex 8000 Programmable Logic Device Family", pages 361-363 (June 1999)
	D	DeHon, Andre, "Reconfigurable Architectures for General-Purpose Computing", Ph.D. Thesis, MIT (Abstract), 368 pages (August 1996)
	E	Fujii, Taro, et al., "A Dynamically Reconfigurable Logic Engine With a Multi-Context/Multi-Mode Unified-Cell Architecture", *IEEE International Solid-State Circuits Conference*, pages 364-365, page 479 (Feb 1999)
	F	Goldstein, S. Copen, et al., "PipeRench: A Reconfigurable Architecture and Compiler", in *IEEE Computer*, Vol. 33, No. 4, pages 70-77 (April 2000)
	G	John, L. K. et al., "A Dynamically Reconfigurable Interconnect For Array Processors", ieee Transactions on Very Large Scale Integration (VLSI) Systems", *IEEE, INC.*, Vol. 6, No. 1, pages 150-157
	H	Levine, Benjamin A., et al., "PipeRench: Power and Performance Evaluation of a Programmable Pipelined Datapath", Hot Chips 14, Palo Alto, CA (August 2002)
	I	Sassatelli, G., et al., "Highly Scalable Dynamically Reconfigurable Systolic Ring-Architecture for DSP Applications", *PROCEEDINGS DESING, AUTOMATION AND TEST IN EUROPE* (March 2002)
	J	Tau, Edward, et al., "A First Generation DPGA Implementation", in proceedings of the Third Canadian Workshop on Field-Programmable Devices, pages 138-143 (May 1995)
	K	JTAG; Test Technology Standards Committee "IEEE Std. 1149.1 Standard Test Access Port and Boundry-Scan Architecture", Institute of Electrical and Electronics Engineers (October 1993)

Examiner	Date Considered

Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include a copy of this form with the next communication to applicant.